#6/Amdt & Appeal 6/26/03

AUS9-1999-0711-US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Fariborz Assaderaghi, et al.

Serial No: 09/964,127

Filed: September 26, 2001

FOR: METHOD FOR PRODUCING AN INTEGRATED CIRCUIT

Group Art Unit: 2822

Examiner: Jeff Vockrodt

Via Facsimile: 703-872-9318

Mail Stop Non Fee Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FIRST OFFICE ACTION

This paper is submitted in response to the Office Action mailed March 28, 2003, in the above-identified application, and is filed within the three-month shortened statutory period for response set in the Office Action.

Please amend the application as follows:

IN THE DISCLOSURE

1. Replace the paragraph beginning at page 1, line 5 with the following paragraph:

The present application is a divisional of U.S. Patent Application Serial No. 09/435,872, filed November 8, 1999, entitled "DECOUPLING CAPACITOR STRUCTURE AND METHOD FOR MAKING AN INTEGRATED CIRCUIT CAPACITOR," now U.S. Patent No. 6,320,237. The Applicants claim priority from this parent application under 35 U.S.C. §120. This parent application is related to the following U.S. Patent Applications:

(1) Application Serial No. 09/435,867, filed November 8, 1999, entitled "METHOD, APPARATUS, AND PROGRAM PRODUCT FOR LAYING OUT CAPACITORS IN AN INTEGRATED CIRCUIT," and

(2) Application Serial No. 09/435,863, filed November 8, 1999, entitled "ON-CHIP DECOUPLING CAPACITOR ARRANGEMENT PROVIDING SHORT CIRCUIT PROTECTION."

The disclosure of the parent application and each of these related applications is incorporated herein by this reference.

2. Replace the paragraph beginning at page 10, line 7 with the following paragraph:

The fabrication steps for producing bulk capacitor structure 10 illustrated in Figures 1 through 5 includes first implanting N-well structure 15. This step corresponds to the N-well formation step used elsewhere in the chip for various devices, and comprises masking areas other than the desired N-well areas and implanting N-type dopant material by a suitable method. As shown particularly in Figure 2, the device body 17 comprises a portion of this N-well, N^+ material.

Similarly formed N-well material makes up P-type transistor bodies (first type transistor bodies) elsewhere on the chip. In alternate forms of the invention, an additional mask and implantation step may be performed just for the area in which each device body 17 will reside. This additional mask/implant step may be performed either immediately before or after the step of producing the N-wells and comprises implanting further N-type impurities in areas which will form a device body 17. Although this additional mask/implantation step reduces the resistivity of the device body 17 and thereby increases the frequency response of the capacitor structure 10 and allows improved area efficiency, the step represents an additional fabrication step for the chip 11.

3. Replace the paragraph beginning at page 10, line 22 with the following paragraph:

With N-well 15 and device body 17 formed, the fabrication method next includes applying thin dielectric layer 28 and then the material for anode 30. These steps correspond to the steps of applying the gate insulation layer and gate electrode material, respectively, in transistor devices elsewhere on chip 11, and are performed concurrently with those steps. The areas other than the areas of chip 11 where lateral regions 20 and 22, and first end region 24 are to be located, are then masked off and N-type impurities are implanted in the exposed areas to form these regions. This step corresponds to the step of producing the source and drain regions in N-type transistor structures (second type transistor structures) at other locations on chip 11 and is performed concurrently with that step. It will be appreciated that the silicon oxide layer previously deposited over the entire chip surface preferably remains in place during the formation of lateral regions 20 and

22, and first end region 24. The N-type impurity may be driven through the thin silicon oxide layer to be implanted in the underlying N-well silicon. However, alternative fabrication arrangements may remove the thin oxide layer or perform other steps at this point such as producing lightly doped regions corresponding the lightly doped drain regions formed in transistor structures on chip 11.

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ATTORNEYS AT LAW

SPECIALIZING IN PATENT, TRADEMARK, COPYRIGHT AND TRADE SECRET LAW

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TELECOPY MESSAGE

TO: EXAMINER JEFF VOCKRODT

FROM: RUSSELL D. CULBERTSON

RE: SERIAL NO. 09/964,127

OUR FILE NO.: AUS9-1999-0711-US2 (2470)

DATE: JUNE 19, 2003

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MESSAGE:

RE: SERIAL NO. 09/964,126
GROUP ART UNIT: 2822

RESPONSE TO OFFICE ACTION MAILED MARCH 28, 2003

PLEASE DELIVER IMMEDIATELY TO
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Thank you!

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